714/ d.5. tal
data error
correction

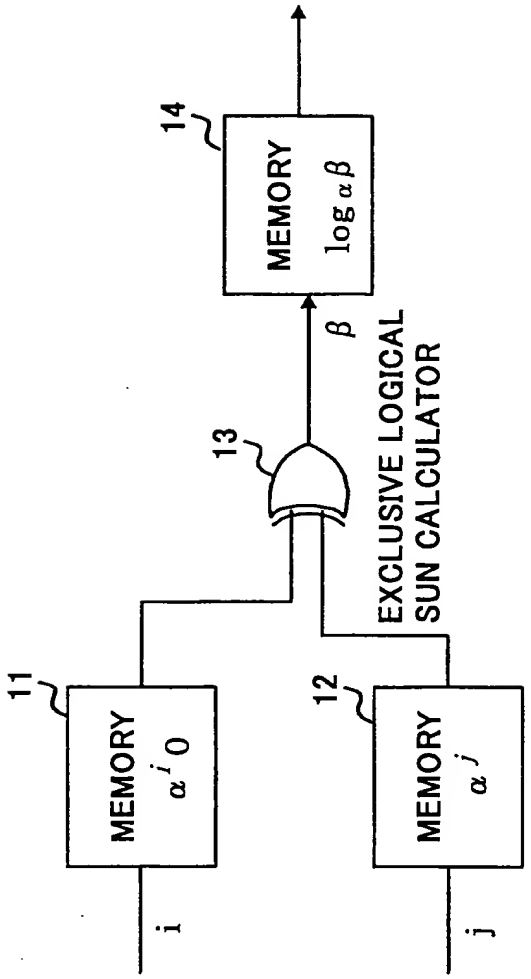

FIG.1

POWER EXPRESSION β	VECTOR EXPRESSION	$\log_\alpha \beta$
α^0	100	0
α^1	010	1
α^2	001	2
α^3	110	3
α^4	011	4
α^5	111	5
α^6	101	6
$\alpha^7(0)$	000	(7)

FIG.2

i \ j	0	1	2	3	4	5	6	7	i_0
0	7	3	6	1	5	4	2	0	0
1	6	4	7	5	1	3	0	2	2
2	4	6	3	2	0	7	1	5	5
3	5	2	1	6	7	0	3	4	4

FIG.3A

i \ j	0	1	2	3	4	5	6	7	i_0
0	7	3	6	1	5	4	2	0	0
2	4	6	3	2	0	7	1	5	5
1	6	4	7	5	1	3	0	2	2
3	5	2	1	6	7	0	3	4	4

FIG.3B

i \ j	0	1	2	3	4	5	6	7	i_0
0	7	3	6	1	5	4	2	0	0
2	20	22	19	18	16	23	17	21	5
1	14	12	15	13	9	11	8	10	2
3	29	26	25	30	31	24	27	28	4

FIG.3C

[7、20、14、29、3、22、12、26、6、19、15、25、1、18、13、5、
16、9、4、23、11、24、2、17、8、27、0、21、10、28]

FIG.3D

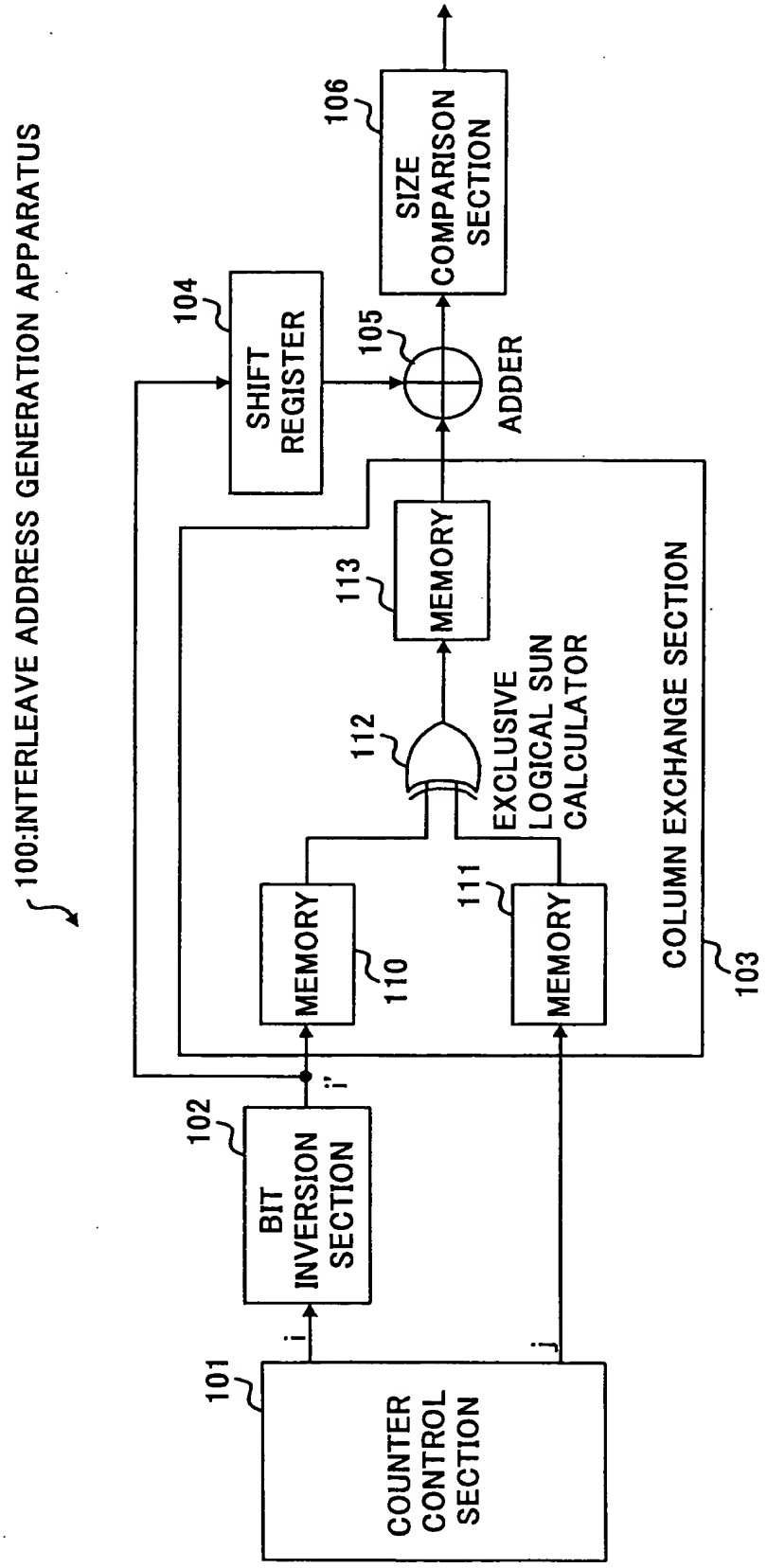
100:INTERLEAVE ADDRESS GENERATION APPARATUS
101
COUNTER CONTROL SECTION
i
j
102
BIT INVERSION SECTION
i'
MEMORY
110
111
MEMORY
112
EXCLUSIVE LOGICAL SUN CALCULATOR
113
MEMORY
COLUMN EXCHANGE SECTION
103
104
SHIFT REGISTER
105
ADDER
106
SIZE COMPARISON SECTION

FIG.4

MEMORY 110

INPUT i 1 DECIMAL	io	OUTPUT α^{io}
0 0 (0)	0	(1, 0, 0)
1 0 (2)	2	(0, 0, 0)
0 1 (1)	5	(1, 1, 1)
1 1 (3)	4	(0, 1, 1)

MEMORY 111

INPUT i	OUTPUT α^{i}
0 0 0 (0)	(1, 0, 0)
0 0 1 (1)	(0, 1, 0)
0 1 0 (1)	(0, 0, 1)
0 1 1 (3)	(1, 1, 0)
1 0 0 (4)	(0, 1, 1)
1 0 1 (5)	(1, 1, 1)
1 1 0 (6)	(1, 0, 1)
1 1 1 (7)	(0, 0, 0)

MEMORY 113

INPUT	OUTPUT
(0, 0, 0)	7
(0, 0, 1)	0
(0, 1, 0)	1
(0, 1, 1)	3
(1, 0, 0)	2
(1, 0, 1)	6
(1, 1, 0)	4
(1, 1, 1)	5

FIG.5

i	i''	j	α^{io}	α^{j}	$\alpha^{io}+\alpha^{j}$	$\log\alpha(\alpha^{io}+\alpha^{j})$	AFTER OFFSET ADDITION
0	0	0	(1, 0, 0)	(1, 0, 0)	(0, 0, 0)	7	7+8×0=7
1	2	0	(1, 1, 1)	(1, 0, 0)	(0, 1, 1)	4	4+8×2=20
2	1	0	(0, 0, 1)	(1, 0, 0)	(1, 0, 1)	6	6+8×1=14
3	3	0	(0, 1, 1)	(1, 0, 0)	(1, 1, 1)	5	5+8×3=29
0	0	1	(1, 0, 0)	(0, 1, 0)	(1, 1, 0)	3	3+8×0=3
1	2	1	(1, 1, 1)	(0, 1, 0)	(1, 0, 1)	6	6+8×2=22
2	1	1	(0, 0, 1)	(0, 1, 0)	(0, 1, 1)	4	4+8×1=12
3	3	1	(0, 1, 1)	(0, 1, 0)	(0, 0, 1)	2	2+8×3=24

FIG.6

09/857022

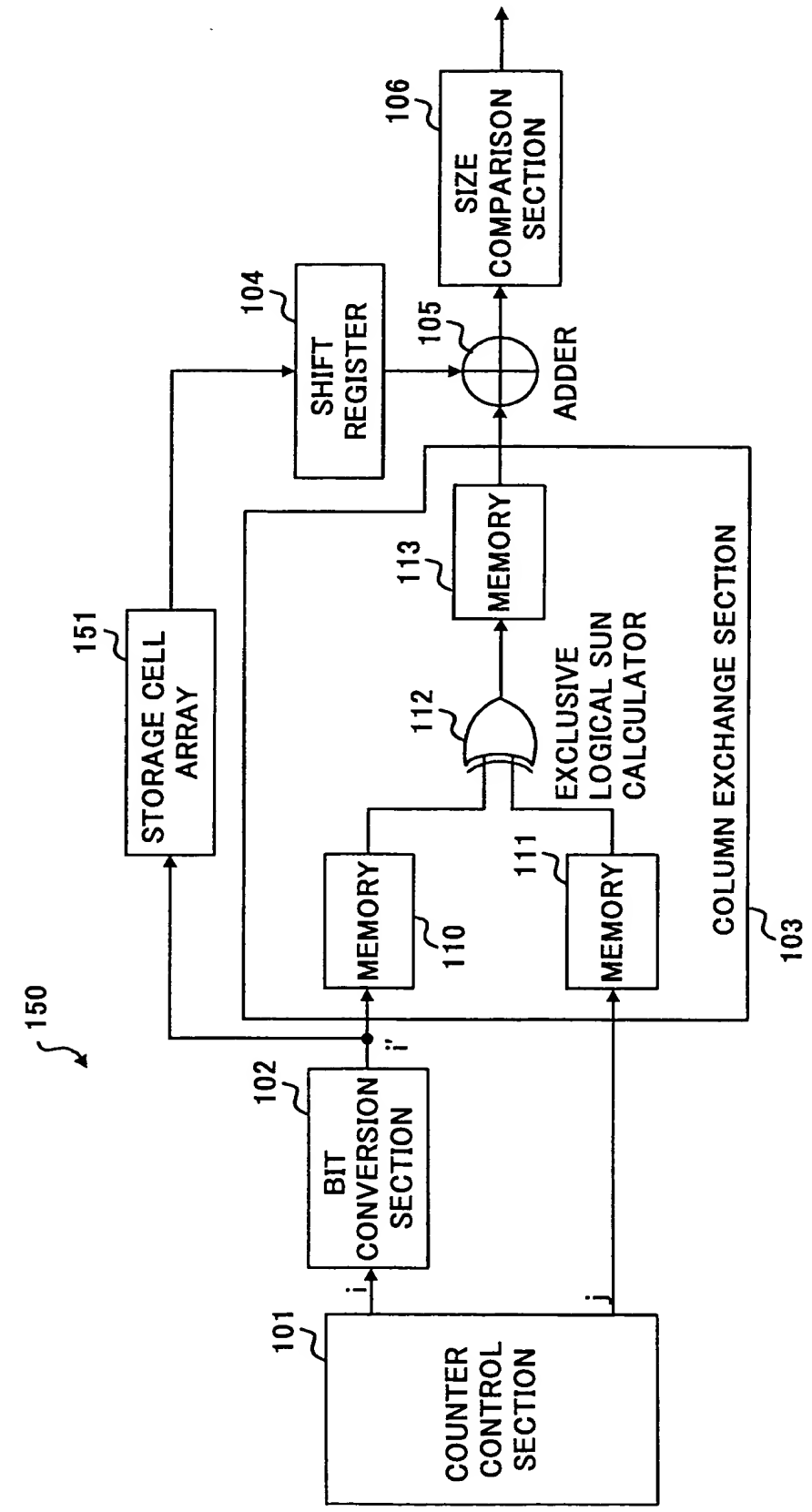
150
101
COUNTER CONTROL SECTION
102
BIT CONVERSION SECTION
i
i'
j
151
STORAGE CELL ARRAY
104
SHIFT REGISTER
105
ADDER
106
SIZE COMPARISON SECTION
110
MEMORY
111
MEMORY
112
EXCLUSIVE LOGICAL SUN CALCULATOR
113
MEMORY
103
COLUMN EXCHANGE SECTION

FIG.7

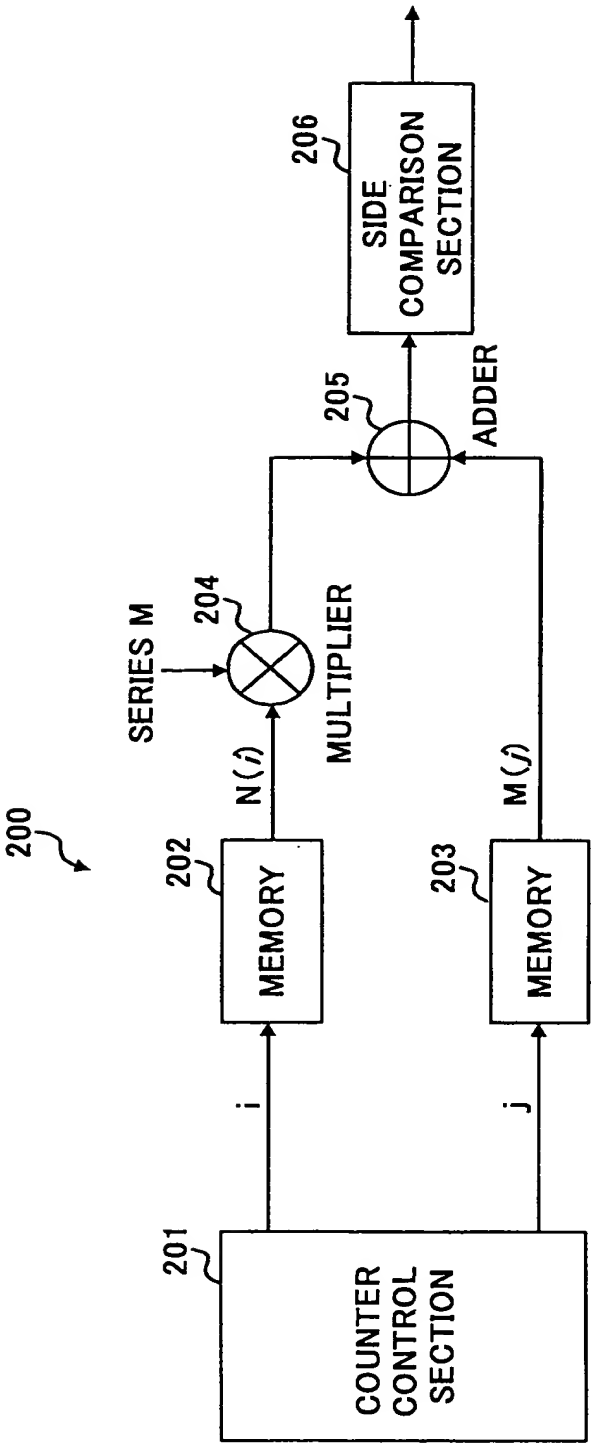

FIG.8

i	N(*i*)
0	2
1	3
2	0
3	1

FIG.9

j	M(*j*)
0	3
1	6
2	4
3	2
4	1
5	5
6	7
7	0

FIG.10

i	0 1 2 3 0 1 2 3 0 • • • • 0 1 2 3
j	0 0 0 0 1 1 1 1 2 • • • • 7 7 7 7

FIG.11A

N(*i*)	2 3 0 1 2 3 0 1 2 • • • • 2 3 0 1
M(*j*)	3 3 3 3 6 6 6 6 4 • • • • 0 0 0 0

FIG.11B

ADDITION RESULT	19 27 3 11 22 30 6 14 20 • • • • 23 31 7 15

FIG.11C

INTERLEAVE ADDRESS	19 27 3 11 22 6 14 20 28 • • • • 8 23 7 15

FIG.11D

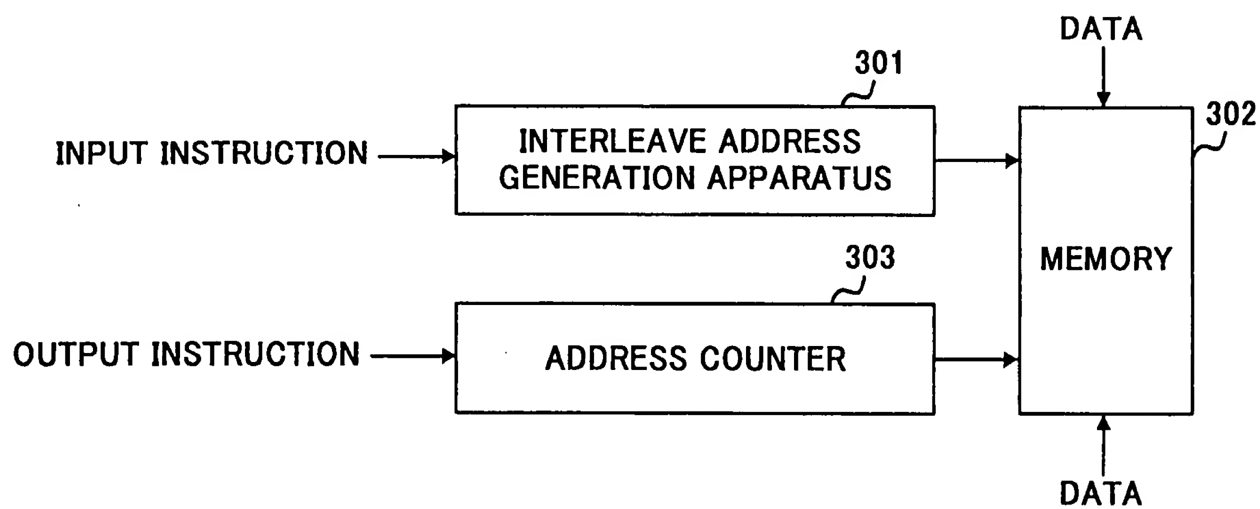

FIG.12

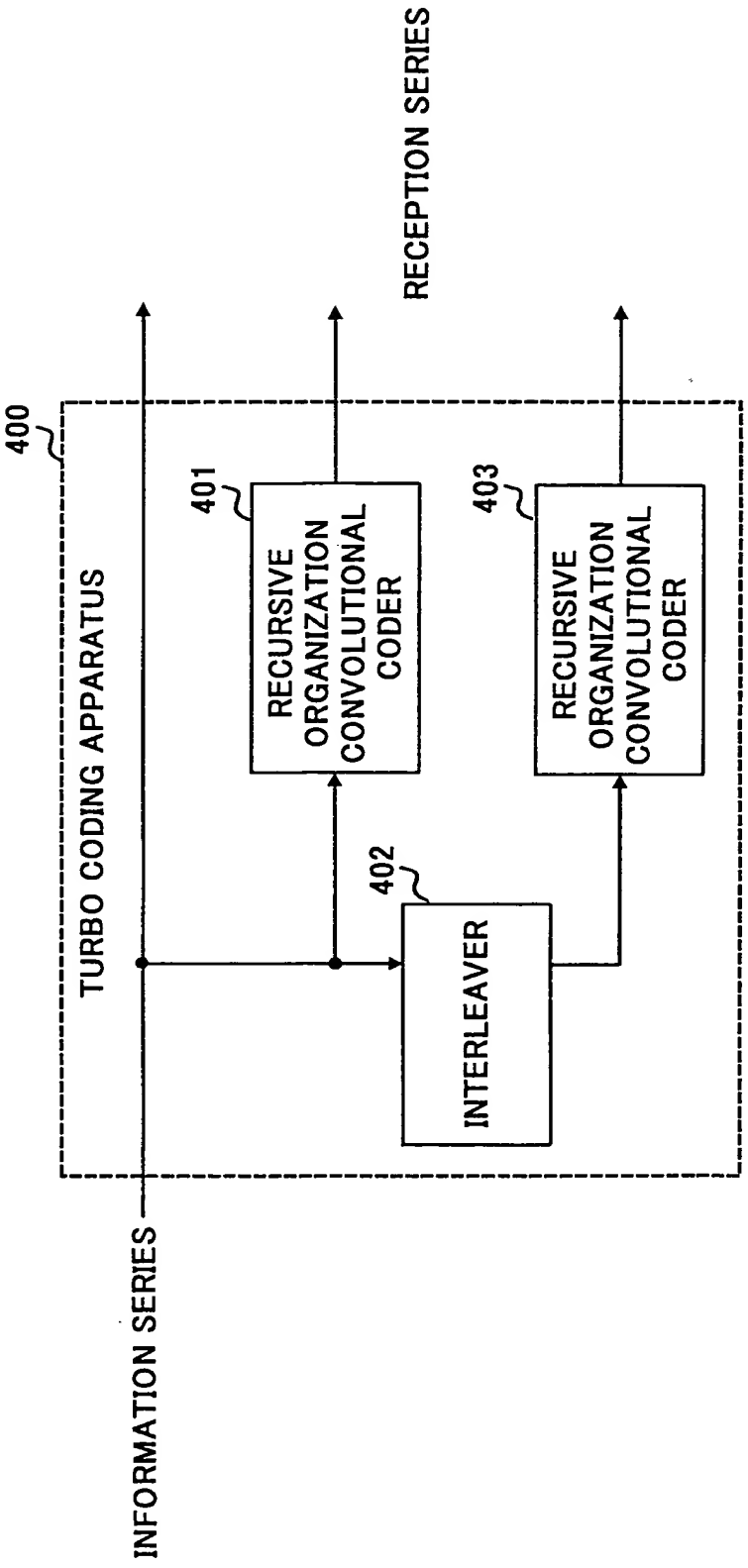

FIG.13

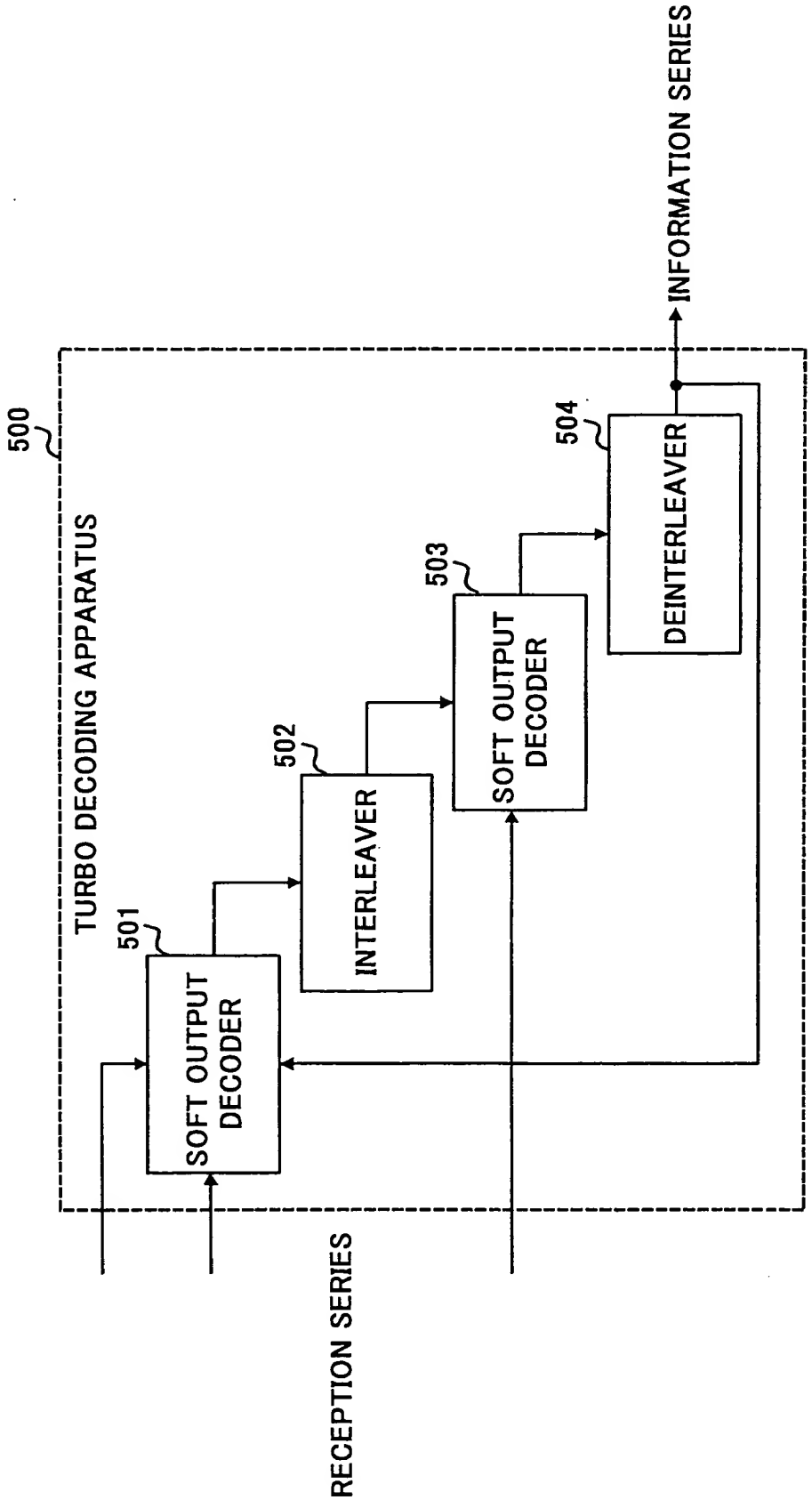
500
TURBO DECODING APPARATUS
501
SOFT OUTPUT DECODER
502
INTERLEAVER
503
SOFT OUTPUT DECODER
504
DEINTERLEAVER
INFORMATION SERIES
RECEPTION SERIES

FIG.14

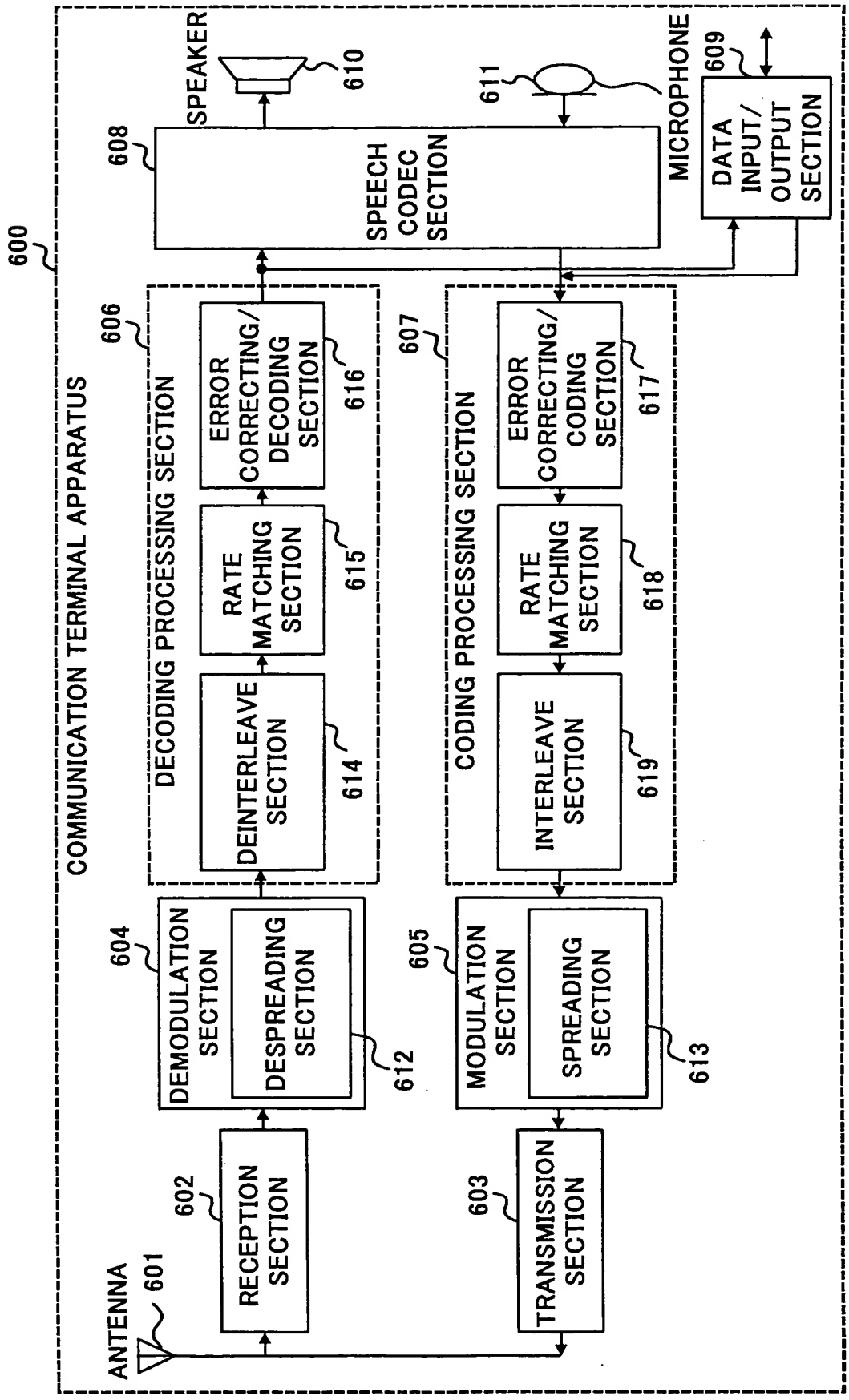
600
COMMUNICATION TERMINAL APPARATUS
ANTENNA
601
602
RECEPTION SECTION
603
TRANSMISSION SECTION
604
DEMODULATION SECTION
DESPREADING SECTION
612
605
MODULATION SECTION
SPREADING SECTION
613
606
DECODING PROCESSING SECTION
DEINTERLEAVE SECTION
614
RATE MATCHING SECTION
615
ERROR CORRECTING/ DECODING SECTION
616
607
CODING PROCESSING SECTION
INTERLEAVE SECTION
619
RATE MATCHING SECTION
618
ERROR CORRECTING/ CODING SECTION
617
608
SPEECH CODEC SECTION
SPEAKER
610
MICROPHONE
611
609
DATA INPUT/ OUTPUT SECTION

FIG.15

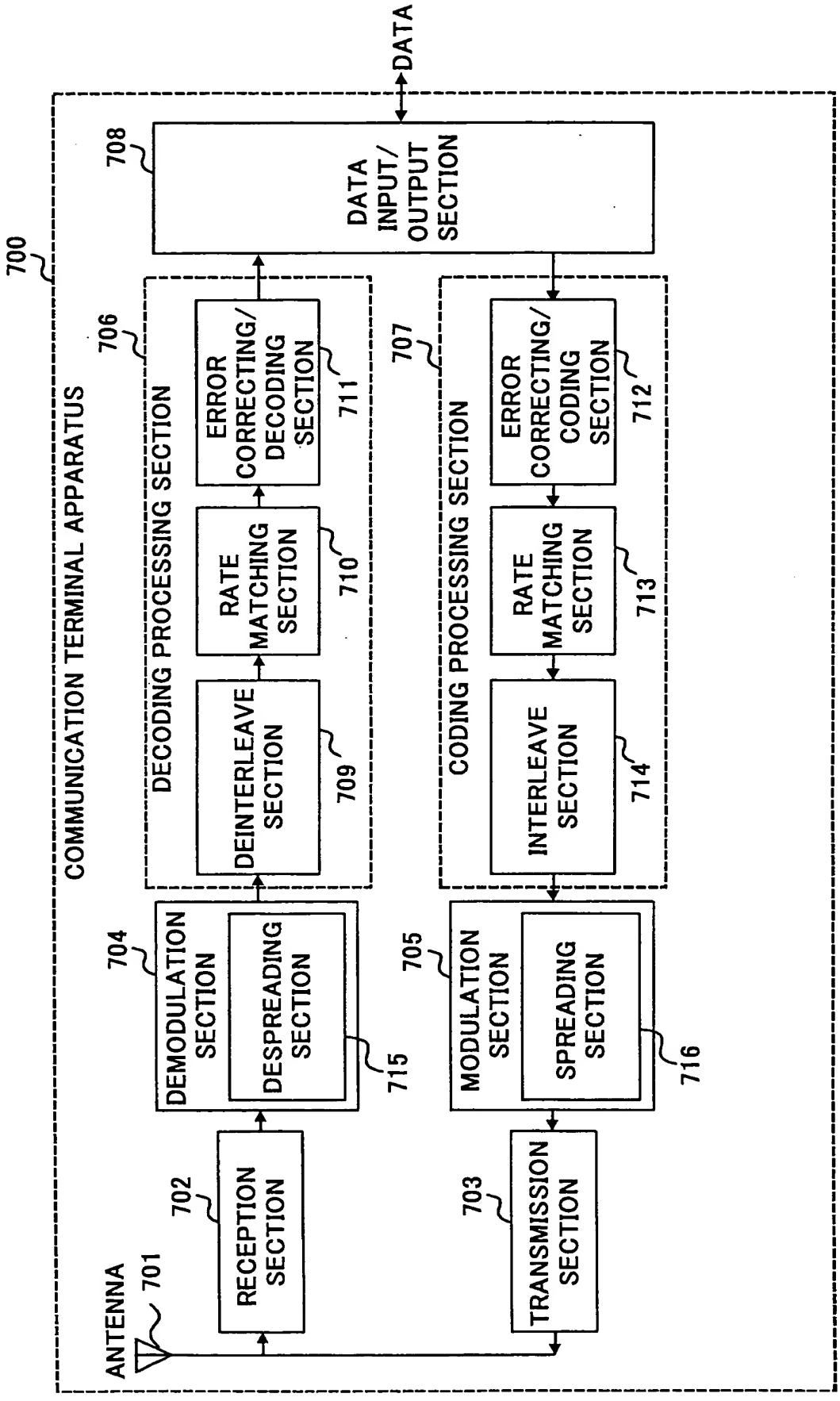
DATA
700
COMMUNICATION TERMINAL APPARATUS
708
DATA INPUT/ OUTPUT SECTION
706
DECODING PROCESSING SECTION
707
CODING PROCESSING SECTION
ERROR CORRECTING/ DECODING SECTION
711
RATE MATCHING SECTION
710
DEINTERLEAVE SECTION
709
ERROR CORRECTING/ CODING SECTION
712
RATE MATCHING SECTION
713
INTERLEAVE SECTION
714
704
DEMODULATION SECTION
DESPREADING SECTION
715
705
MODULATION SECTION
SPREADING SECTION
716
ANTENNA
701
702
RECEPTION SECTION
703
TRANSMISSION SECTION

FIG.16